

# Nonlithographic Nano-Wire Arrays: Fabrication, Physics, and Device Applications

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**Abstract**—A novel system of nanostructures is described consisting of nonlithographically produced arrays of nano-wires directly electrodeposited into porous anodic aluminum oxide templates. Using this method regular and uniform arrays of metal or semiconductor nano-wires or nano-dots can be created with diameters ranging from  $\sim 5$  nm to several hundred nanometers and with areal pore densities in the  $\sim 10^9$ – $10^{11}$   $\text{cm}^{-2}$  range. We report on the present state of their fabrication, properties, and prospective device applications. Results of X-ray diffraction, Raman and magnetic measurements on metal (Ni, Fe) and semiconductor (CdS, CdSe,  $\text{CdS}_x\text{Se}_{1-x}$ ,  $\text{Cd}_x\text{Zn}_{1-x}\text{S}$  and GaAs) wires are presented. The  $I$ - $V$  characteristics of two terminal devices made from the nano-arrays are found to exhibit room temperature periodic conductance oscillations and Coulomb-blockade like current staircases. These observations are likely associated with the ultra-small tunnel junctions that are formed naturally in the arrays. Single-electron tunneling (SET) in the presence of interwire coupling in these arrays is shown to lead to the spontaneous electrostatic polarization of the wires. Possible device applications such as magnetic memory or sensors, electroluminescent flat-panel displays, and nanoelectronic and single-electronic devices are also discussed.

## I. INTRODUCTION

SEMICONDUCTOR technology has advanced to the point where it is now possible to create devices incorporating one-dimensional confinement (quantum wells, or 2-D structures). Today, submicron lithography in combination with a variety of production techniques such as MBE and MOCVD is routinely used to fabricate quantum devices with novel characteristics.

This situation contrast with that prevailing in the area of one- and zero-dimensional structures. Although a number of successful efforts have been reported, e.g., the fabrication of free-standing Si or Se nano-wells or nano-pillars, the established lithographic techniques seem to have approached their technological and economic limits, making the cost of controllably manufactured 1-D and 0-D structures prohibitively high as the dimensions of individual structural units fall to the 10–100 nm range, especially when high-density nano-arrays are needed. These challenges have forced many

to look for new approaches to nano-manufacturing, especially ones which grow nanostructures directly rather than those depending on material removal. For example, one might write the desired structure directly on the semiconductor surface using a focused ion beam or a scanning probe microscope (AFM or STM [1]). Such methods look promising for making devices in small batches, but become unrealistic when a large area or a large throughput are needed.

An alternative approach is to make use of self-organization, i.e., the spontaneous formation of nanostructures that can occur naturally under specific conditions. One rapidly evolving strategy along these lines is to exploit the formation of semiconductor islands in the planar growth of certain lattice-mismatched semiconductor systems. By carefully adjusting the material systems and growth conditions one can get more or less ordered 2-D arrays of nano-sized clusters [2]–[4]. This method, although promising in some cases such as quantum-dot laser fabrication [3], is limited in terms of the possible range of material systems and with regard to the dimensions of the nano-islands achievable.

Another, and, in a certain sense, contrasting approach, is the direct nano-fabrication by selective deposition in the openings of a self-organized template. In this case the size and shape of the nano-objects are controlled by the size and shape of the openings in the nanotemplates, and may vary over a wide range depending on the template used. This flexibility also extends to the range of materials deposited in the template's openings. This approach is particularly attractive since it circumvents the lithographic limitations altogether by making use of naturally occurring nanotemplates. Examples of such nanotemplates are zeolites and molecular sieves [5], polymer nuclear track membranes [6], or porous anodic aluminum oxide (AAO) films [7], [8].

In choosing a template one must take into account its stability, its insulating properties, the minimal size, density and uniformity of the pores as well as the ability to integrate the template into a device or chip. The latter includes the ability to form a good quality template film on a desired substrate and to make electrical contact to the nanostructures incorporated within the template. An attractive candidate from this point of view is AAO which has a highly oriented porous structure (Fig. 1) with very uniform and nearly parallel pores [9] that can be organized in an almost precise hexagonal structure [10].

In this paper, we will discuss our work with what we believe to be one of the most promising of the existing nonlithographic

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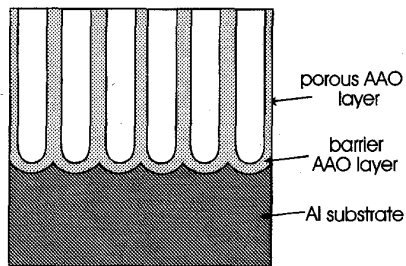


Fig. 1. Idealized cross section of porous anodic aluminum oxide.

fabrication methods—the electrochemical deposition of metals and semiconductors into porous AAO films. Currently, we are able to produce densely-packed, uniform, 2-D nano-pore arrays in AAO with pore diameter,  $d_p$ , ranging from 4 to 200 nm, pore length from 1 to 50  $\mu\text{m}$ , and pore density in the  $10^9$ – $10^{11}$   $\text{cm}^{-2}$  range. The smallest pore diameter we are able to make at present is of the order of or smaller than the Bohr diameters of some bulk semiconductor excitons, suggesting that quantum size effects should be observed. Moreover, the use of AAO templates readily allows scale-up to very large surface area systems and is amenable to continuous production.

Providing that AAO is formed on a conductive substrate, electrochemical (EC) methods, which can be used to grow materials of a wide range of morphologies, structures and composition, seem to be a logical choice for selective deposition into the pores. Electrodeposition (ED) has previously been used successfully for the formation of ceramic [11], metallic [12], and semiconductor [13] superlattices. Attempts were also made to use sequential under potential electrodeposition of monolayers to grow epitaxial compound semiconductor films [14].

Electrodeposition of metal nano-wire arrays in porous aluminum oxide has been used to produce deposits with interesting magnetic [14], [15], catalytic [16], and optical properties [17], at times differing from those of the bulk metals. The wires faithfully reproduce the shape of the pores [18]. Other porous films such as polymeric membranes, have also been used for the ED of ferromagnetic Ni and Co [19] as well as for multilayered Cu–Co [20] nano-wires. A similar approach was also used to deposit 200-nm diameter cadmium selenide/telluride micro-wires in the pores of commercially available AAO membranes [21]. However, the large pore diameter of those templates preclude the fabrication of wires displaying quantum size effects.

This paper summarizes our progress in making the AAO nanotemplates and various nanostructures, as well as in exploring some of the interesting physics and device applications which these nanostructures promise. In Sections II and III, we describe the technique for fabricating nano-arrays and present experimental results illustrating effects ascribable to anisotropy, electron confinement and room temperature single electron tunneling (SET) in nano-wire based devices. In Section IV, we outline a theoretical analysis of the effect of interwire coupling on the SET characteristics in such systems [22]. Finally, we discuss, preliminarily, some device

applications and research directions which the new method and structures may make possible.

## II. NANO-WIRE ARRAYS AND DEVICES FABRICATION

### A. Nano-Wire Deposition and Characterization

The procedure for preparing porous AAO films with varying pore diameters is well established [7]. After the porous AAO template is fabricated, AC electrolysis is used to deposit metals (Ni, Co, Fe, and others) and semiconductors (CdS, CdSe,  $\text{CdS}_x\text{Se}_{1-x}$ ,  $\text{Zn}_x\text{Cd}_{1-x}\text{S}$ , and GaAs) into the pores resulting in the formation of nano-wire arrays contained in an oxide matrix. For metals and for GaAs the electrodeposition was carried out at room temperature while for the  $\text{A}^{\text{II}}\text{B}^{\text{VI}}$  systems it was carried out at 100–180  $^\circ\text{C}$ . During electrodeposition the temperature of the electrolyte was maintained to within 0.5  $^\circ\text{C}$ . Metals and GaAs were deposited out of aqueous acidic electrolytes, whereas,  $\text{A}^{\text{II}}\text{B}^{\text{VI}}$  were deposited from solutions containing the metal salt ( $\text{CdCl}_2$ ,  $\text{ZnCl}_2$ ) and the elemental chalcogen (S, Se) dissolved in dimethylsulphoxide [23]. Iron nano-wires were deposited in an electrolyte consisting of 120 g/l of  $\text{FeSO}_4 \cdot 7\text{H}_2\text{O}$ , 45 g/l  $\text{H}_3\text{BO}_3$  and 0.5 g/l ascorbic acid. Methods for depositing other semiconductors are currently being developed. To improve crystallinity some samples were annealed under oxygen-free  $\text{N}_2$  for 1 h at 500  $^\circ\text{C}$ .

The electrodeposited metal and semiconductor nano-wires were examined using electron microscopy by first liberating them from their AAO matrix by dissolving the anodic oxide in 0.1 M NaOH at 40  $^\circ\text{C}$  (Fig. 2) then detaching the particles from the film surface and suspending them in water to form a fairly stable colloid. Electron microphotographs suggest that the deposited material fills the pores uniformly.

*CdS Wires:* Deposition of CdS was carried out in a solution containing 0.055M  $\text{CdCl}_2$  and 0.19M elemental sulphur in DMSO [23] at 30–50 V(rms) of AC current (60 Hz) applied between the Al\AAO working electrode and a graphite counter electrodes for 5–60 min, depending on the template parameters [24]. Quantitative electron microprobe analysis indicates a 1:1 stoichiometry to within the detection tolerance of the technique. X-ray diffraction (XRD) profiles of the AAO\CdS arrays correspond to the hexagonal phase of CdS. No unreacted Cd or S was detected.

The XRD data suggest that the spatial confinement of the deposition affects the crystallite orientation. The relative intensity of the (002) diffraction peak of the AAO\CdS is considerably higher than those recorded for CdS electrodeposited on Pt or for polycrystalline CdS powder, indicating that in AAO the hexagonal crystallites grow with the  $c$ -axis oriented along the pore (Fig. 3). Annealing improves the diffraction pattern of AAO\CdS only slightly while preserving its texture. The contribution of other primary diffraction planes [(100), (101), and (110)] is suppressed.

Before annealing, the unit cells of AAO\CdS deposited in templates with varying pore diameters were found to be compressed in comparison with that of the polycrystalline hexagonal CdS standard. The interplane spacing,  $d_{002}$ , of as deposited samples shows a nonmonotonic dependence on

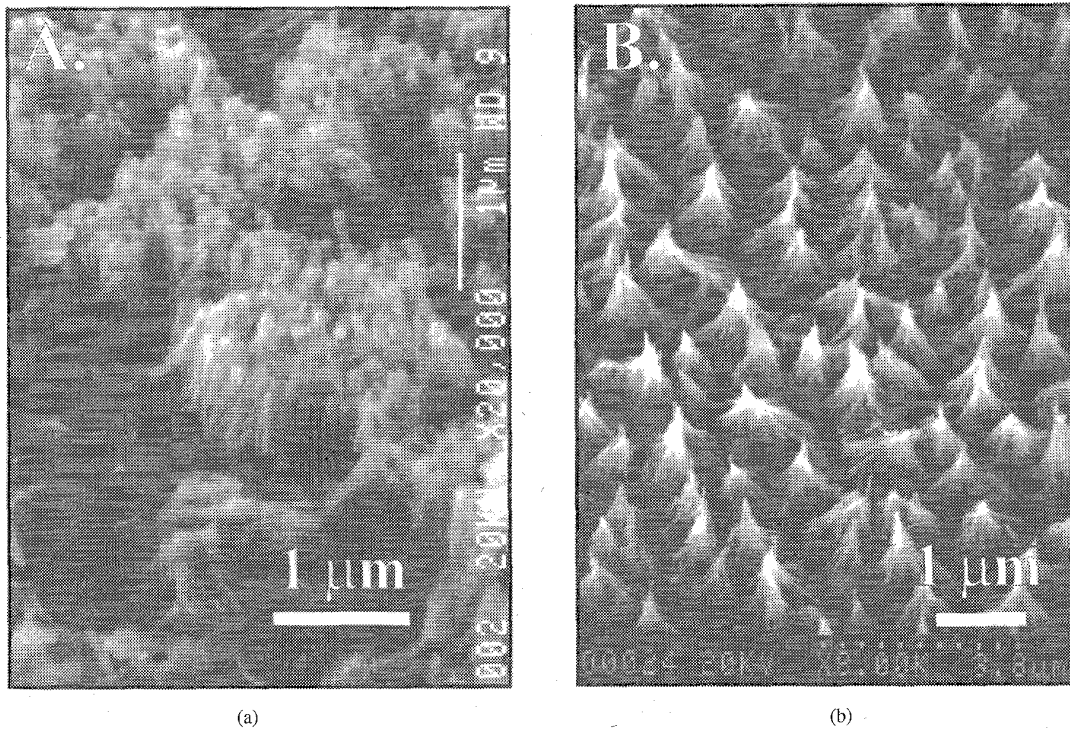


Fig. 2. SEM micrographs of (a) CdS, and (b) Fe nano-wires, exposed by the dissolution of the AAO matrix.

diameter (Fig. 4). Annealing relieves this lattice distortion to some extent, leaving a slight residual increase in  $d_{002}$  with nano-wire diameter (Fig. 4).

The linear dimension of the crystalline domains along the [002] axis,  $D_{002}$ , determined for annealed samples using the Scherrer equation relating the mean coherence length to the XRD peak width, increases with nano-wire diameter in the  $8 \text{ nm} \leq d_p \leq 15 \text{ nm}$  range becoming almost constant for  $d_p > 15 \text{ nm}$  (Fig. 4). This indicates that the growth constraint is less pronounced for larger pores.

We propose that the spatial constraint to growth imposed by the walls of the pores is the main factor determining the observed structural features of the AAO\CdS samples, especially its texture. A more thorough analysis of the AAO\CdS nano-wire crystalline structure was reported elsewhere [24].

**CdS<sub>x</sub>Se<sub>1-x</sub> and Cd<sub>x</sub>Zn<sub>1-x</sub>S Wires:** One strategy for fabricating AAO\semiconductor nano-wire arrays with tuneable band gap energies is to deposit ternary semiconductors. The possibility for doing this is illustrated with the CdS<sub>x</sub>Se<sub>1-x</sub> and Cd<sub>x</sub>Zn<sub>1-x</sub>S system. Deposition of CdS<sub>x</sub>Se<sub>1-x</sub> was carried out in a solution containing 0.055 M CdCl<sub>2</sub> and 0.19 M of the elemental chalcogens (Se and S) in DMSO. In order to vary the Se/S ratio in the nano-wire solutions with Se/S ratios ranging from 20:1 to 1:20 were used. Deposition of Cd<sub>x</sub>Zn<sub>1-x</sub>S was carried out in a solution contained 0.055 M (CdCl<sub>2</sub>+ ZnCl<sub>2</sub>) and 0.19 M elemental S in DMSO. The Cd/Zn ratio was varied to obtain the desired metal ratio in the nano-wire. For these compounds the optimal deposition parameters are quite different from those for CdS nano-wires. Under the same conditions (deposition temperature,  $t_d$ , and voltage,  $U_d$ ) the reaction of Cd with Se was found to be much slower than

with S (Fig. 5). As a result, we increased  $t_d$  [Fig. 5(a)] and decreased  $U_d$  [Fig. 5(b)], thereby increasing CdSe formation and decreasing the deposition of Cd metal so as to obtain a stoichiometric deposit. These two parameters were then optimized for a wide range of the electrolyte compositions (Se/S = 0.05–20) to produce pure semiconductor phases. Annealing is also helpful in ensuring that the reaction between Cd and Se is complete. It also promotes the completion of the formation of stoichiometric phases. The co-deposition of ZnS with CdS was found to occur only at high deposition voltage (50 V). Likewise the various phases of Cd<sub>x</sub>Zn<sub>1-x</sub>S could only be produced with high deposition temperatures. The composition of the electrolytes (S/Se or Zn/Cd ratios) determines the nano-wire composition, with XRD pattern changing from that of hex-CdS to that of hex-CdSe (Fig. 6) or ZnS. For un-annealed CdS<sub>x</sub>Se<sub>1-x</sub> lower than standard values of  $d_{002}$  were observed due to the aforementioned lattice distortion.

**GaAs Wires:** The lack of sufficient information in the literature [25] on the electrochemical deposition of GaAs prompted us to study the effect of the Ga(III)/As(III) ratio and pH on the deposition of GaAs from aqueous electrolytes. For pH < 2.5 no GaAs is deposited. Arsenic is found to be the main deposited component under those conditions on Pt, ITO, or AAO substrates, and H<sub>2</sub> evolution was the primary side reaction. This is in agreement with the fact, that Ga electrodeposition is possible only at pH > 2.5 at the onset of hydrolysis [26].

With solutions of 0.05 M of Ga(III) at pH = 2.5 and Ga(III)/As(III) = 2/1 a reddish-yellow sample was generated which produced resonance Raman spectra with a well

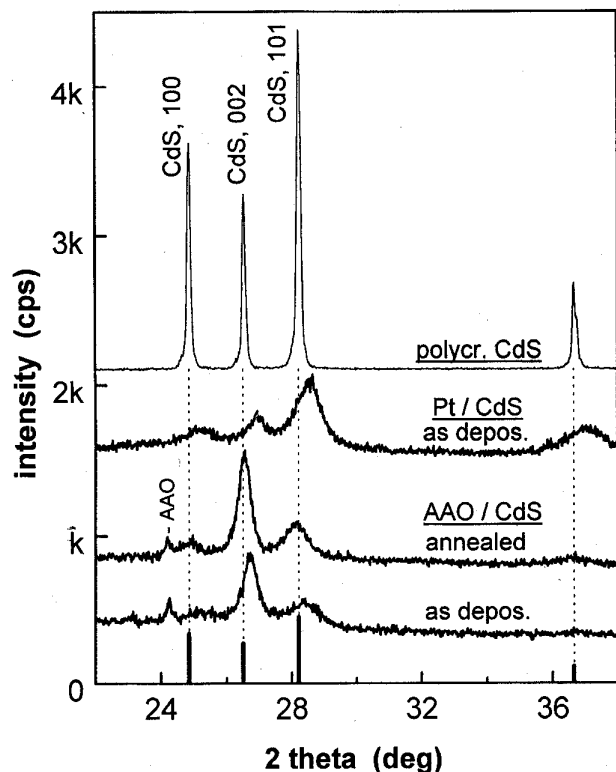


Fig. 3. X-ray diffractograms of as deposited and annealed AAO\CdS nano-wire array (mean wire diameter 35 nm, length 0.8  $\mu\text{m}$ ), Pt\CdS film electrodeposited under the same conditions (1- $\mu\text{m}$  thickness) and polycrystalline CdS. Diffraction line position and relative intensity of hexagonal CdS standard (ASTM #6-314) are shown as vertical lines.

defined peaks at approximately  $280\text{ cm}^{-1}$  characteristic of GaAs (Fig. 7). However, XRD did not reveal crystalline GaAs, probably due to the small quantity of the deposited material and its rapid oxidation. Samples lost their colors over a period of several hours.

### B. Device Fabrication

The AAO templates allow one to manipulate the nano-wires arrays and to incorporate them into a variety of potential designs of nano-devices [27]. In Fig. 8, we illustrate some of the fabrication steps possible. Following anodization (Step I.1) and optional pore widening (Step I.2), metal or semiconductor (SC) electrodeposition (Steps II.1–3) produces the array of the nano-wires. The composition of the wires can be modulated at this stage along its length, resulting in the formation of p-n junction or heterojunctions (II.3). The next step (III.1) is the partial etching of the AAO template to expose the nano-wire tips for further processing. Steps III-2a–5a, 2b–3b, and 2c–4c illustrate several processing strategies at this stage:

- 1) Nano-wire array with contacts to one (tip emitters, III.4a) or both (III.5a) ends;
- 2) Nano-wire array sandwiched between two insulating tunneling junctions (III.3b);
- 3) Array of the metal\SC nano-heterojunctions (anti-dot array, III.4c).

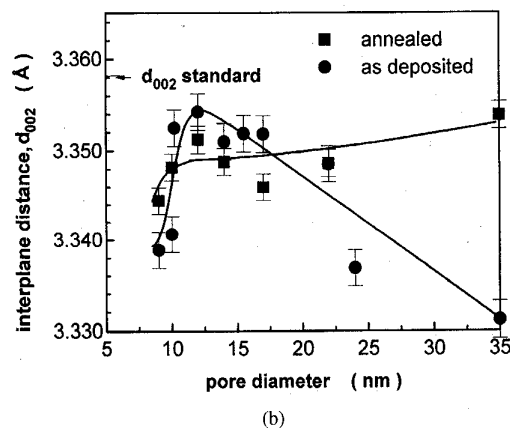
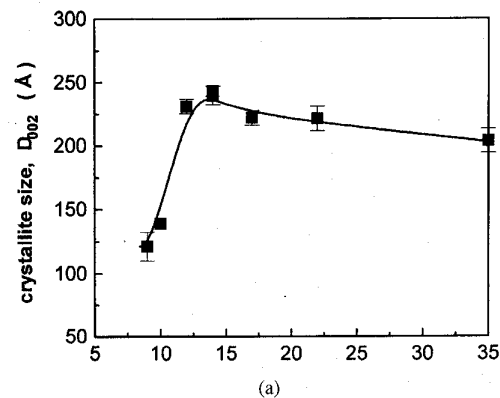


Fig. 4. Crystalline domain size,  $D_{002}$ , and interplanar distance,  $d_{002}$ , of AAO\CdS as a function of the pore diameter.

The fabrication may include 1) deposition of contacts to the wires (Steps III.2a, 5a, 3b, 3c) by vacuum evaporation (Ag, Au) or DC plasma sputtering (transparent conductive indium-tin oxide); 2) Al substrate and barrier layer of AAO etching (Steps III.3–4a) to access the other end of the wires; and 3) chemical or electrochemical deposition of the insulator (Step III.3b) or semiconductor (Step III.2c). Based on these and other processing technologies, one can develop a variety of devices utilizing the nano-wire arrays.

## III. PROPERTIES OF THE METAL AND SEMICONDUCTOR NANO-WIRE ARRAYS

### A. Band Gap Engineering in Semiconductor Nano-Wires

*Size Effect in CdS Nano-Wires:* Polarized resonance Raman spectroscopy (RRS) was used to investigate qualitatively the effect of the nano-wire diameter on the band gap energy of the CdS quantum wires. The Bohr diameter of the 1S exciton of CdS (4 nm, [28]) is close to the smallest AAO pore diameter that we can produce. Accordingly, some indication of quantum confinement effects should be observable in these particles.

The measured RRS spectra are dominated by overtones of the longitudinal optical LO phonon (Fig. 9). The overall intensity of the Raman scattering and the number of the ob-

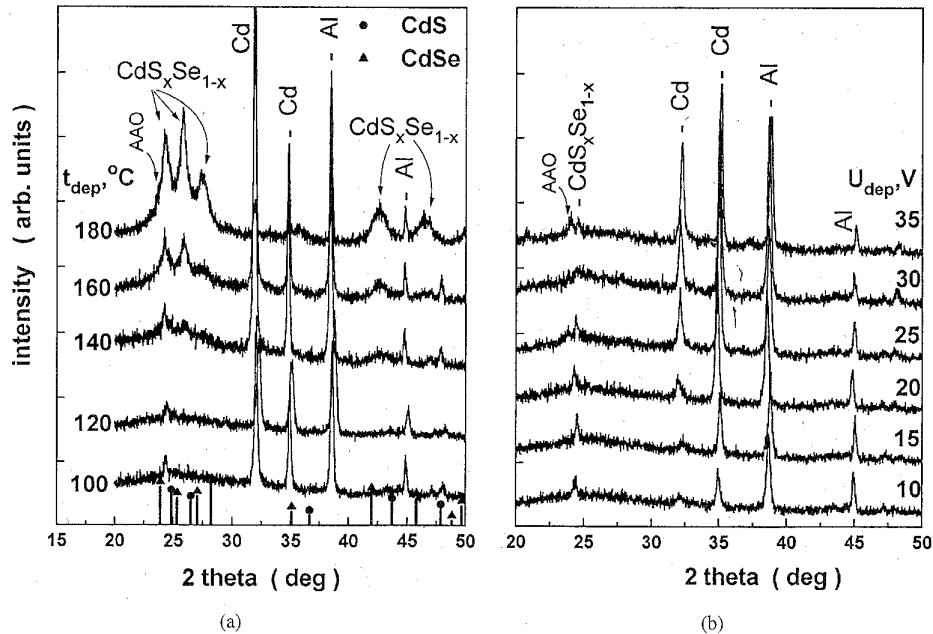


Fig. 5. X-ray diffractograms of As deposited AAO/CdS<sub>x</sub>Se<sub>1-x</sub> nano-wire arrays (mean pore diameter 35 nm) as a function of (a) deposition temperature,  $t_d$ , and (b) deposition voltage,  $U_d$ . Vertical lines are CdS (ASTM #6-314) and CdSe (ASTM #8-495) standards.

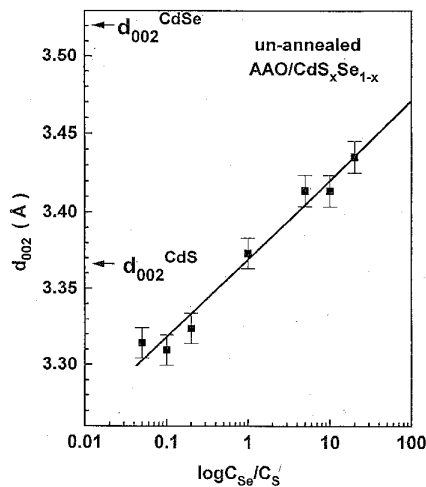


Fig. 6. Interplanar spacing,  $d_{002}$ , of the (002) diffraction planes of AAO/CdS<sub>x</sub>Se<sub>1-x</sub> nano-wire arrays (mean pore diameter 35 nm) as a function of Se/S ratio in the electrolyte.

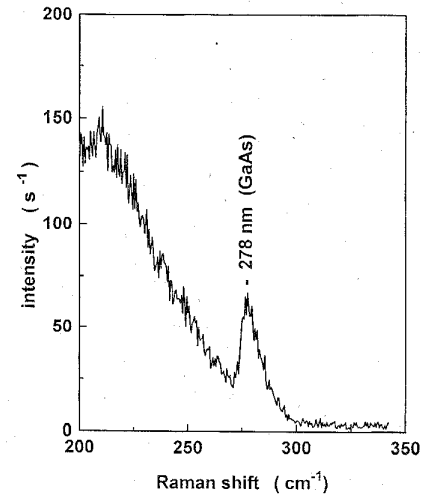


Fig. 7. Resonance Raman spectrum of AAO/GaAs, excited with 514-nm 200-mW Ar<sup>+</sup>-laser light.

served overtones increase dramatically with annealing, making quantitative analysis possible [29]. This behavior is probably due to the fact that the intensities of the RRS lines are very sensitive to any improvement in the crystallinity of the wires. Furthermore, the intensity of the Raman scattering might also benefit from the annealing of the interfaces or grain boundaries.

The intensities of the overtones in the Raman spectra of semiconductor clusters depend strongly on the particle diameter [29], [30], and are related to the value of the band gap. Polarized RRS of AAO/CdS nano-wires excited with

the electric field vector both along and across the wires showed that the ratio of the first overtone intensity to that of the fundamental mode decreases with decreasing wire diameter, suggesting that the quantum size effect regime has been approached (Fig. 9). Based on this dependence we calculated [29] band gap energies and other parameters by fitting experimental data to the expression which describes the ratios of the overtone intensities as a function of excitation energy. The derivation of the formulas is given in details in [29] and [30].

The exciton energies determined with RRS polarized across the long axis of the wires ranged from 2.376 eV for the large

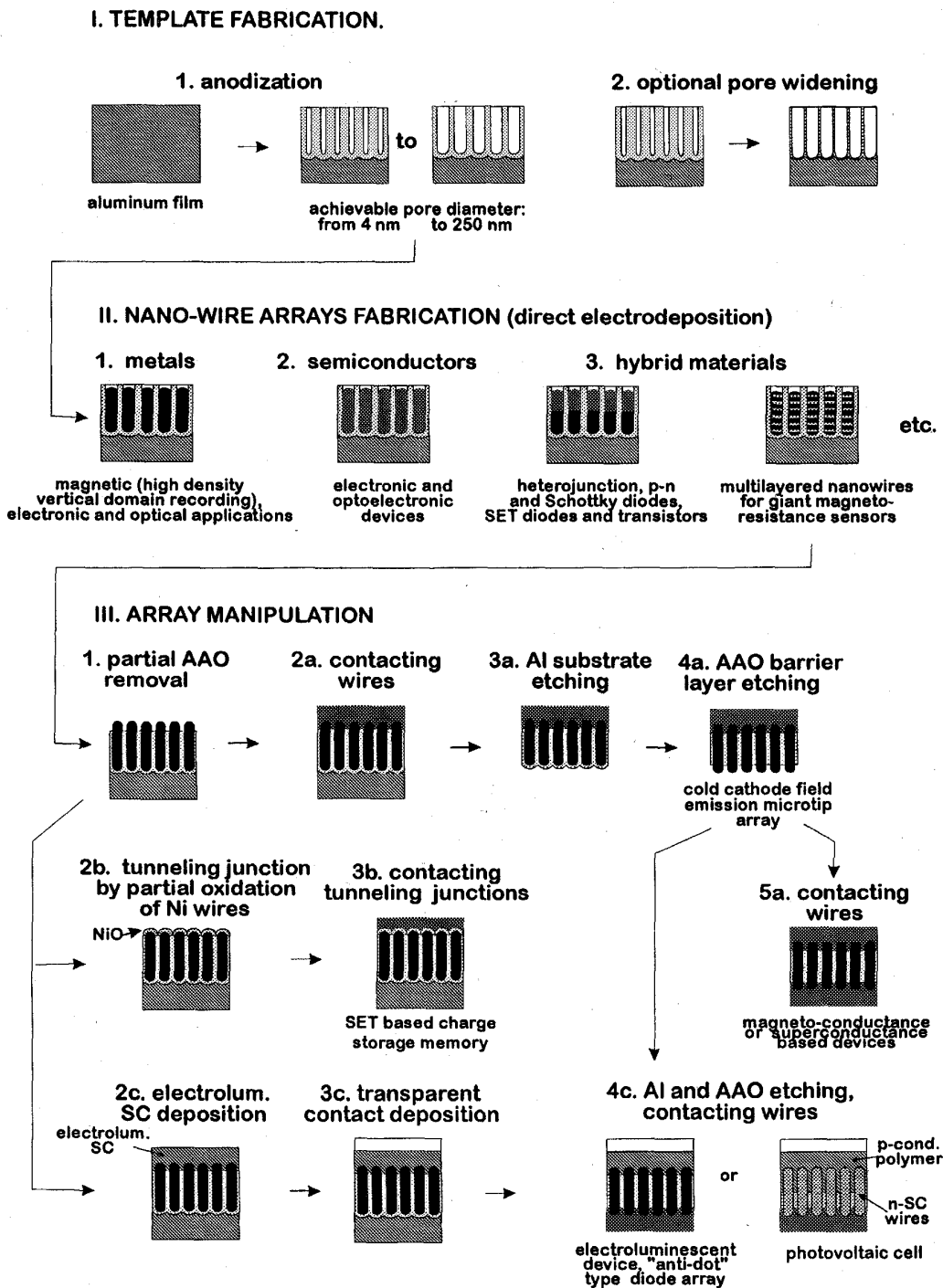


Fig. 8. Processing steps in the fabrication of nano-wire arrays and device prototypes.

pore diameters to 2.417 eV for the smallest pore diameter and are well behaved as a function of the nano-wire diameter (Fig. 10) following a functional dependence on the cross-sectional radius of the wire similar to that developed for spherical particles [31]. Bulk values for the effective masses of the electron and hole and the optical dielectric constant were used and the band-gap energy of bulk CdS was determined to

be 2.42 eV by measuring the optical absorption of a 22-nm nano-wire sample.

*B. Compositional Band Gap Tuning*

The control over ternary semiconductor, e.g.,  $CdS_xSe_{1-x}$ , composition allowed us to produce nano-wire arrays with widely varying values of the optical band gap. Normalized

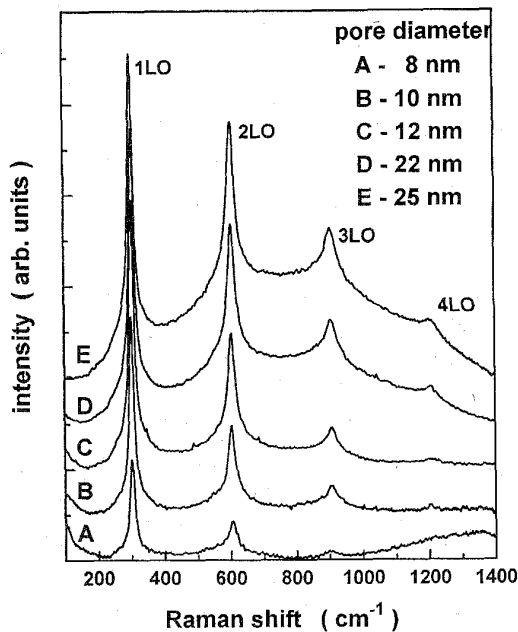


Fig. 9. Resonance Raman spectra of AAO/CdS nano-wire arrays with the polarization of the excitation laser beam and the collected light across the wires (ss-polarization).

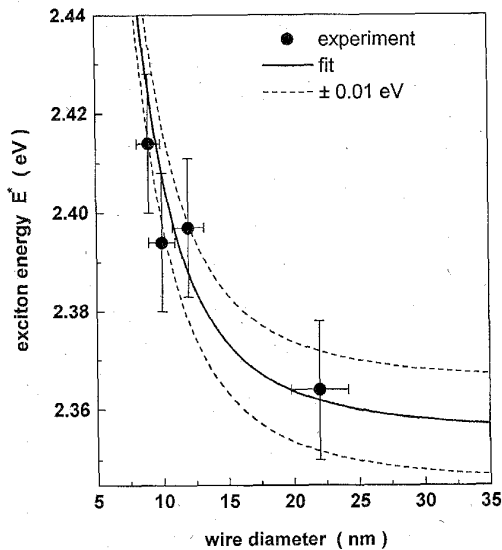


Fig. 10. Exciton energy as a function of mean diameter of CdS nano-wires. Points are the experimental values, solid curve is the fit based on the Kayanuma's calculation [31].

absorption spectra of AAO/CdS<sub>x</sub>Se<sub>1-x</sub> as a function of Se/S ratio in electrolyte (Fig. 11) illustrate this. A variation of this technique can be used to produce nanoscale heterojunction wires.

### C. Ferromagnetic Nano-Wires and Novel Magnetic Materials

The fact that AAO templates could be used to prepare arrays of closely spaced ferromagnetic wires or needles oriented appropriately for use as perpendicular magnetic recording

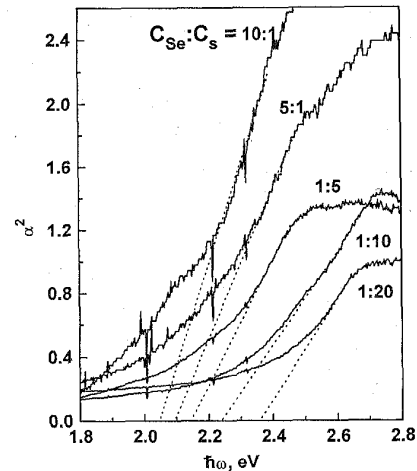


Fig. 11. The square of the absorption,  $\alpha^2$ , versus  $\hbar\omega$  for AAO/CdS<sub>x</sub>Se<sub>1-x</sub> nano-wire arrays (mean pore diameter 35 nm) as a function of the Se/S ratio in the electrolyte. The linear portions are extrapolated to estimate the band gap of the CdS<sub>x</sub>Se<sub>1-x</sub>.

media was recognized [14] by our group and by a number of Japanese workers, especially Kawai [14]. Among its beneficial characteristics, AAO based magnetic materials can incorporate zero-valent ferromagnetic metals such as Fe, Ni, and Co, or their alloys into the oxide matrix, so that materials with very large coercivities and very high levels of saturation magnetization can be created. Normally, for reasons of stability, one uses metal oxides since under normal circumstances small metallic particles oxidize rapidly, often forming nonmagnetic oxides. The difference with AAO lies in the fact that metal needles deposited in the pores of the AAO film can be subsequently sealed using a simple chemical procedure. The resulting oxide matrix is stable and impervious to oxygen allowing the metal to remain in its unoxidized state. Samples produced this way have been kept in room air for several years without obvious deterioration. Secondly, by choosing appropriate conditions one can create extremely anisotropic materials which possess their greatest magnetic moments in the direction perpendicular to the surface, ideally suited for perpendicular recording. The extremely small size and good orientational uniformity of the particles deposited in the pores, and our ability to create materials with a wide range of particle aspect ratios and areal densities means that one can create materials with almost any desired magnetic characteristics either for magnetic storage applications or as a vehicle for studying the magnetic properties of fine particles under extremely controllable conditions.

As an example, we describe results obtained with the same ferromagnetic material (Fe) deposited in anodic oxide films prepared in phosphoric and oxalic acid films. The minimum pore diameter achievable by anodizing in phosphoric acid was 50 nm and in oxalic acid -12 nm. The pores of the AAO templates were widened so as to increase, in turn, the diameters of the metal wires deposited in them thereby varying the aspect ratio. The anodized aluminum was subjected to AC electrolysis in an appropriate Fe(II) containing electrolyte

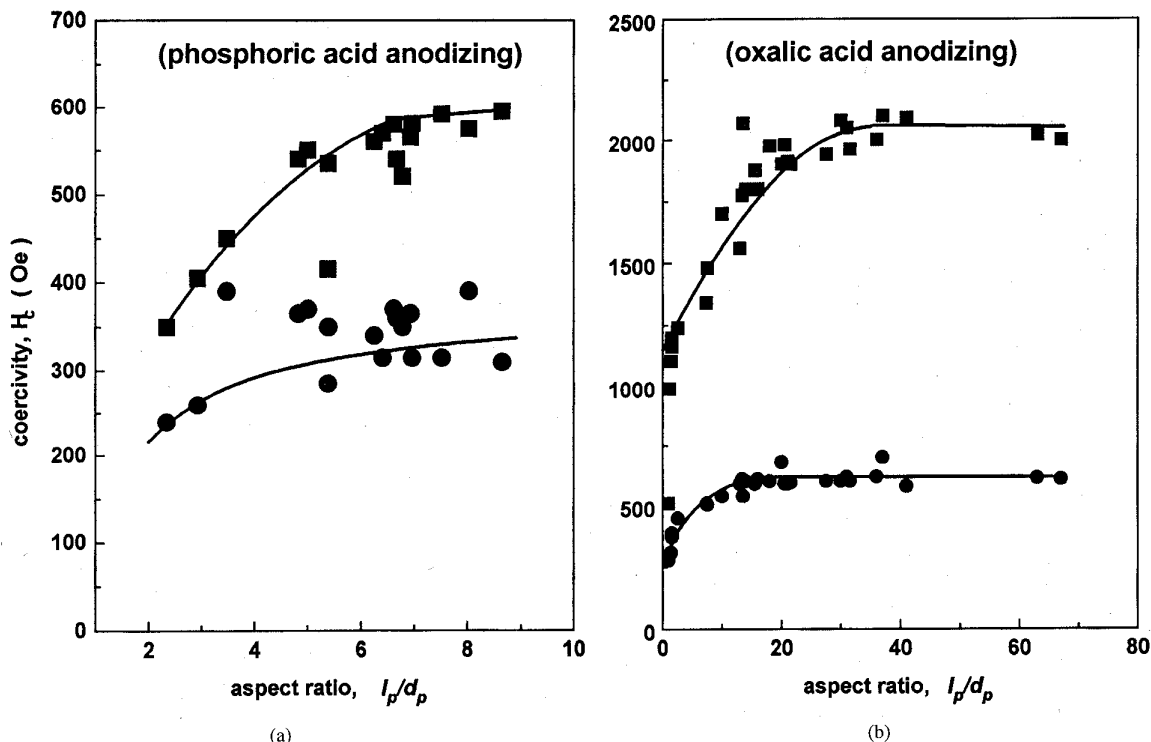


Fig. 12. Measured perpendicular,  $H_{c\perp}$ , and parallel,  $H_{c\parallel}$ , coercivities of AAO/Fe nano-wires as a function of the mean aspect ratio of the wires for (a) AAO formed in phosphoric acid, and (b) AAO formed in oxalic acid. Squares— $H_{c\perp}$  circles— $H_{c\parallel}$ .

for various lengths of deposition times,  $\tau_d$ , resulting in the deposition of iron needles of various average lengths and aspect ratios [15].

The coercivity as a function of metal particle aspect ratio is shown in Fig. 12. The upper set of points refer to measurements carried out with the magnetic field aligned along the axis of the iron nano-wires (i.e., along the surface normal of the film), while the lower set of points was recorded with the magnetic field aligned across the wire axes. The results illustrate the anisotropy of the magnetic properties—the mean coercivity perpendicular to the surface was approximately  $1.6\times$  that along the surface for phosphoric films [Fig. 12(a)] and  $4.6\times$ —for oxalic films [Fig. 12(b)]. It also illustrates our ability to vary the magnetic properties of the sample by controlling the dimensional parameters of the constituent iron wires. The functional dependence of  $H_c$  on the aspect ratio suggested that the metal deposit consists of a cylindrical assembly of fused single-domain particles [15].

The coercivities achieved with iron loaded oxalic acid AAO templates [15] were considerably higher than that for iron wires in phosphoric acid AAO at equivalent values of the aspect ratios (Fig. 12). Moreover, while the (perpendicular) coercivity achievable with iron loaded into phosphoric films achieves an asymptotic value at approximately 600 Oe, with iron loaded oxalic films the analogous asymptotic value is in excess of 2100 Oe. The reason for this is as yet unresolved, although there is some evidence from the literature that phosphorous incorporation into iron reduces considerably the value of its saturation magnetization. Whatever the reason, this result illustrates that there are controllable parameters other

than size that can be manipulated both to produce materials with desirable and controllable magnetic characteristics and to provide an abundant source of unusual magnetic materials which display a rich and novel physics ripe for investigation.

#### D. Electron Tunneling in Nano-Wires

Room temperature operation of devices based on single-electron tunneling (SET) requires extremely small capacitance tunnel junctions, which are difficult to fabricate lithographically. Using the metal in AAO/nano-wire electrodeposition technique described above we fabricated a two terminal device consisting of a 10-nm nickel nano-wire array sandwiched between metal contact layers (Fig. 8, #6b), with a bottom junction consisting of the barrier oxide layer ( $\sim 10\text{--}20$  nm) and a top junction formed by a thin ( $\sim 8$  Å) nickel oxide film grown on the tips of the nickel nano-wires. The device, which can be considered to be a 2-D array of double junction systems with common “source” and “drain” contacts exhibited very complex  $I$ - $V$  characteristics at room temperature including conductance oscillations, and a current-voltage staircase (Fig. 13). Periodic conductance oscillations were observed in analogous structures with CdS nano-wires (Fig. 14), and recently in Ag/AAO<sub>BL</sub>/Ni-wires/CdS film (Fig. 8, #6c) array devices (Fig. 15), where BL refers to the barrier layer. The origin of the room temperature periodic conductance oscillations, especially of the type shown in Fig. 15 with an extremely small ( $\ll kT/e$ ) period of  $\sim 10$  mV, is still unresolved and raises several fundamental questions. Similar small-period ( $\sim 6$  mV) oscillations had recently been observed in a system with

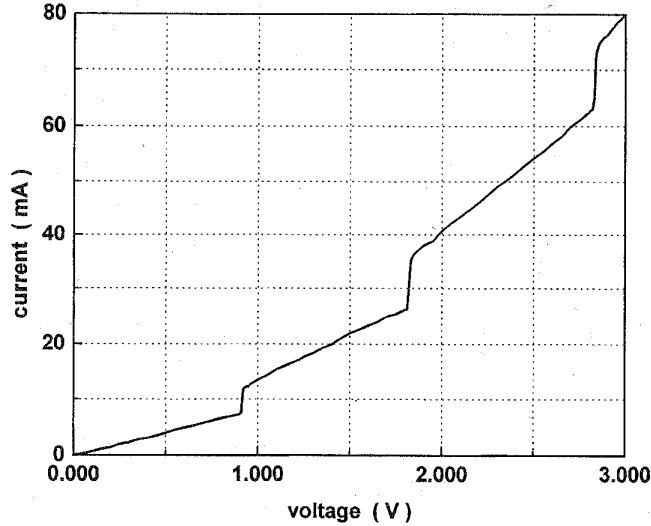


Fig. 13. Current-voltage characteristics of a double tunnel junction array  $\text{Al}/\text{AAO}_{\text{BL}}/\text{Ni-wires}/\text{NiO}/\text{Ag}$  obtained (in the dark) at 300 K.

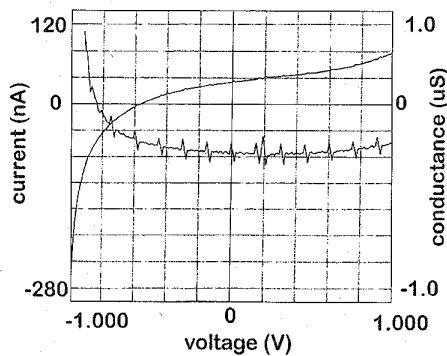


Fig. 14. Periodic conductance oscillations of  $\text{Al}/\text{AAO}_{\text{BL}}/\text{CdS-wires}/\text{Ag}$  array obtained in the dark at 300 K. Mean wire diameter was  $\sim 10$  nm.

somewhat similar geometry, by using a conducting AFM tip placed on a resonant-tunneling diode structure to measure its  $I$ - $V$  characteristics [32].

The  $I$ - $V$  staircase observed with metal wires (e.g., Fig. 13) on the other hand resembles the Coulomb staircase predicted by the standard theory of single-electron tunneling (SET) when the drain-source junctions are very dissimilar [33] and [34]. Simple estimates of the junction capacitances for a single 10-nm diameter wire in the array, yield values in the order of  $10^{-19}$  F (for a  $\sim 20$ -nm aluminum oxide film, bottom junction) to  $10^{-18}$  F (for the  $\sim 8$ -nm nickel oxide film, top junction) [35]. The reasonableness of these estimates, together with the  $\sim 1$  V step width support the suggestion that we are observing SET. However, these arrays are different from those of model systems considered previously [34], where tunneling occurs sequentially in the plane of an array of islands connected in matrix, and the coupling capacitances are of the same order as the junction capacitances. An adequate understanding of the present systems must take into account a number of features unique to them and of effects such as the very strong electrostatic coupling between nano-wires due to the small

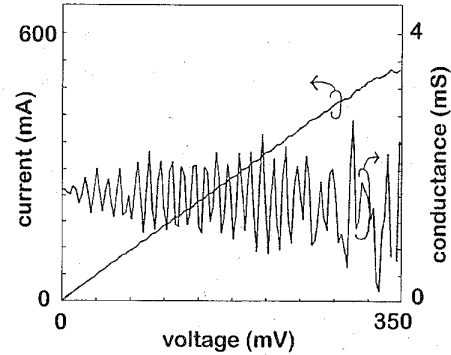


Fig. 15. Room temperature current-voltage characteristics and differential conductance of  $\text{Ag}/\text{Ni-wires}/\text{CdS}/\text{ITO}$  array with a 500-nm CdS layer deposited on top of Ni wires. Mean wire diameter was  $\sim 35$  nm.

inter-wire spacing (20–50 nm) compared to the wire length ( $> 1 \mu\text{m}$  in this case).

#### IV. SINGLE ELECTRON TUNNELING THROUGH COUPLED NANO-WIRES: SPONTANEOUS POLARIZATION

As a first step we investigated some of the effects of interwire coupling on the single-electron tunneling in coupled double junction systems by considering a two wire system [Fig. 16(a)] which can be taken to be a building block of our device [22]. Using the “global rule” of SET [36] to calculate the effect of wire charging on the tunneling probabilities, we performed Monte-Carlo simulations of the electron transport through the system assuming a low-impedance environment. Typical numerical values used in the modeling were: junction capacitances  $C_{ij} = (1.6 \pm 0.2) \cdot 10^{-19}$  F, coupling capacitance  $C_0 = (0-200) \cdot C_{ij}$ , junction resistances  $R_{11} = R_{12} = 50$  k $\Omega$  (source),  $R_{21} = 200 \cdot R_{11}$  and  $R_{22} = (1-100) \cdot R_{21}$  (drain). We assumed zero conductance between wires.

##### A. Results

We first consider an array of weakly-coupled ( $C_0 \ll C_{ij}$ ) double junction systems (which, in analogy with our fabricated samples, we visualize as individual nano-wires capped with oxide layers; however, the analysis is general) for which the overall electron current is simply a sum of the *independent* tunneling currents through the individual system each of which is determined by the applied voltage, and the parameters describing the individual wires. At low enough temperature when the SET conditions are fulfilled, the electrical charge  $N_j$  (in units of electron charge  $e$ ) on each wire is controlled by Coulomb repulsion. For asymmetric junctions this is strictly determined by the applied voltage.

Contrariwise, for very strong coupling ( $C_0 \gg C_{ij}$ ) the whole array responds to each tunneling event as a single double junction system with effective junction capacitances  $C_i = \sum_j C_{ij}$  regardless of the location at which the electron began the tunneling process. In this case, it is mainly the total wire charge  $N = N_1 + N_2$  which determines the tunneling probability, while the effect of the charge on an individual wire is small (of order  $C_j/C_0$ ). An apparent consequence of this is the reduction of the Coulomb-blockade region in proportion

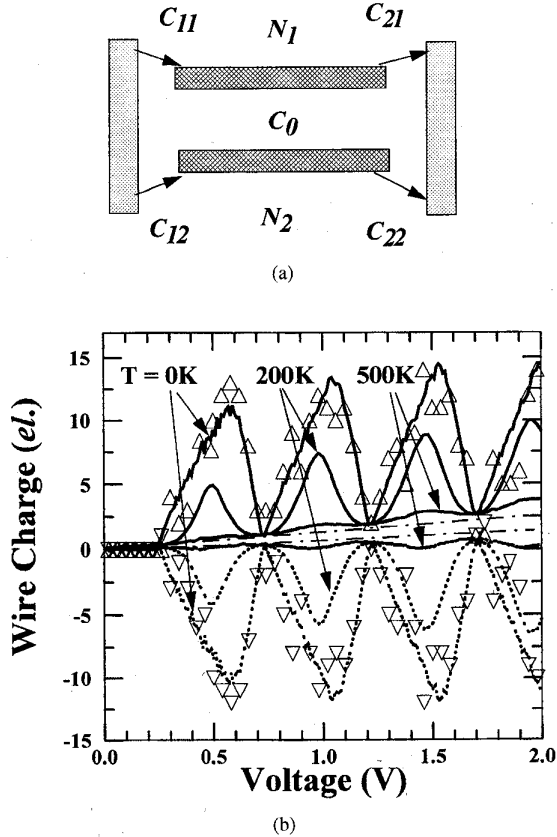


Fig. 16. (a) Two wire double junction system. Arrows show the prevailing directions of tunneling for  $V > 0$ ; (b) average charges on the wire  $\langle N_i \rangle$  versus voltage at three different temperatures. Solid and dotted curves represent the wires with the lower and the higher drain resistances, respectively. The symbols “ $\Delta$ ” and “ $\nabla$ ” indicate the charges on the wires at a particular instant in time for  $T = 0$  K.

to the number of participating wires. Application of this finding directly to our experimental system is difficult since the number of wires actually participating in the charge transport is unknown owing to the dispersion in oxide thickness, and therefore in the junction resistances.

An interesting aspect of strong coupling is the spontaneous polarization of neighboring wires [22], when an accumulation of excessive electrons on one wire is partly compensated by hole accumulation on another. The polarization is conveniently described by the difference in the charges on the individual wires  $P = N_2 - N_1$ . Since the polarization is associated with a very small electrostatic energy  $\sim P^2/8C_0$ , it can be spontaneously created by the shot noise associated with the tunneling current. It can often exceed considerably the total charge  $N$  on both wires, which, at low enough temperatures, remains strictly controlled by the Coulomb repulsion.

The polarization,  $P$ , oscillates stochastically in time around some average value  $\langle P \rangle$ , with  $\langle P \rangle = 0$  when the wires are identical. The polarization becomes more regular for asymmetrical wires, when electrons can tunnel from one of the wires more easily than from the other. In this case, the maximum saturation level is  $\langle P_{\max} \rangle \sim C_0/(C_{11} + C_{21})$  when the ratio of drain resistances  $R_{22}/R_{21} \gg 1$ .

This effect is voltage- and temperature-sensitive. It practically disappears at the critical voltages corresponding to steps in the  $I$ - $V$  curves, when the maximum total charge on both wires  $N$  increases by one. At these points an electron tunneling through the source junction is almost elastic blocking the wire polarization which requires some, although only a small amount of energy, to be created. This phenomenon brings about an oscillatory dependence on the part of the charges  $N_j$ , on the wires, of the average polarization  $\langle P \rangle$  and of the polarization noise  $\langle \Delta P^2 \rangle$  on the applied voltage [Fig. 16(b)].

The strong wire polarization between these critical voltages is a SET-induced effect which does not exist at high temperatures, i.e., when  $kT \geq e^2/2C_j$ , so that thermal fluctuations control the charge statistics. At higher temperatures (500 K-curves in Fig. 16) the average charge on the wires approaches the Kirchhoff value (indicated by the dashed-dotted lines in Fig. 16(b) at all voltages and varies almost linearly with the voltage. For lower temperatures the polarization statistics is governed instead by the shot noise in combination with the Coulomb-blockade effect, which suppresses the fluctuations of the total charge on the two wires but increases the anticorrelated fluctuations of the charges on the individual wires.

What is interesting and counter-intuitive is that not only the average polarization, but also the polarization noise rises as the temperature decreases. This anomalous temperature dependence of the polarization fluctuations is especially striking if the low frequency part of the noise spectrum is considered. Fig. 17 illustrates how a decrease in the spectral bandwidth of the SET-induced polarization noise at lower temperature (which at  $T = 0$  K is determined by the time constant of the coupling capacitor  $\tau_c \sim RC_0$ ) contributes to the increase in the low frequency polarization noise. In excess of a 20-fold increase is observed when the temperature decreases from 300–0 K. The figure also shows a striking contrast at low temperatures between the low frequency noise intensity of the total charge number,  $N$ , and that of the charge polarization,  $P$ ,  $\langle \Delta P^2 \rangle(\omega = 0)$  exceeds  $\langle \Delta N^2 \rangle(\omega = 0)$  by 5 orders of magnitude.

Thus, wire coupling under SET conditions leads to strong inter-wire polarization of the electrical charges on individual wires. For two wires the polarization is found to be stochastic, with its average amplitude and dispersion periodically changing as function of the applied voltage. In the much more complex case of multiwire systems and nano-wire arrays, this SET-induced spontaneous self-polarization may lead to a number of quasistatic and dynamic phenomena, among them the prospect of a phase transition from random to ordered polarization behavior according to the value of the system parameters or of the applied field. Self-sustained polarization waves might also be possible in such systems. That possibility is being investigated.

## V. PROSPECTS OF THE NONLITHOGRAPHIC NANO-WIRE AND NANO-DOT ARRAYS

The phenomenon of SET-induced spontaneous polarization described above, as well as the experimentally observed but not yet well understood room temperature conductance os-

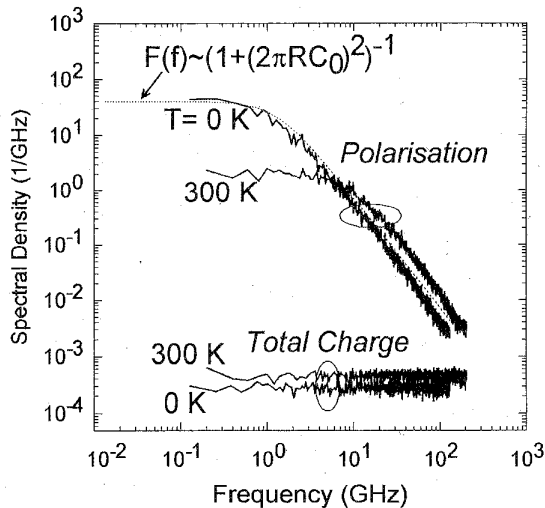


Fig. 17. Spectral density of the fluctuations in the wire charge polarization,  $P$ , and of the total charge on the wire,  $N$ , at  $T = 0$  K and  $T = 300$  K.

cillations in nano-wire/semiconductor structures, are only a few examples of the apparently rich physics possible with systems based upon the nonlithographic nano-wire arrays. We believe that these structures provide novel opportunities for both basic research and device engineering. On the basic research front, they suggest and provide the experimental basis for investigating a variety of collective effects in 2-D or 1-D arrays, as well as an opportunity for studying some intrinsic properties of individual 1-D (or 0-D) objects, among others, carrier localization at low temperatures, magneto-conductivity, superconductivity in low-dimensional structures. This can be accomplished either "on wafer"—e.g., using a conductive AFM tip to locate and electrically access a wire, or by dissolving the template material and working with individual wires directly.

As for device development, the high density, uniformity and very small wire diameter of the arrays suggest applications such as flat-panel electroluminescent displays [37], magnetic [15], [38], and charge storage memories, quantum wire lasers and detector arrays. For the first-mentioned application, the very high electric field, which exists at the wire tips even for relatively low voltages between the wire and a contact layer, can lead to efficient electroluminescence if a thin layer of an appropriate semiconductor is placed between the wires and a transparent contact layer.

In magnetic storage, the nano-wire arrays offer the advantages of perpendicular magnetic anisotropy useful in perpendicular recording, high density, square hysteresis loops, high coercivity and almost quantum read-write characteristics due to the almost single-domain nature of the wires. These structures are also promising for giant magnetoresistance (GMR) sensors with the current perpendicular to the plane (CPP) geometry as an alternative to the in plane (CIP) configuration presently used [39]. CPP does not require as thin a layer as CIP; additionally, control over coercive field is possible by changing the layer thickness and the wires diameter. Antipar-

allel alignment can be produced by depositing magnetic layers with different thicknesses.

Along less traditional directions, the ultra-small capacitance tunnel junctions, which can be produced easily, make these arrays potential candidates for room temperature single-electronics, including arrays of SET diodes and transistors [27]. One can also think of using the nano-wire (or better yet, nano-dot, which result when the wires are made short enough) arrays as charge storage media (analogous to magnetic storage) when operating in the SET regime. Fabrication of highly-ordered nano-arrays [9] should make the information (charge states) carried by individual wires easier to read. This can be accomplished, at least in the laboratory, with AFM read and write tips sensitive to electrostatic forces. Other interesting applications might include single- or few-wire devices such as trans-impedance nano-crosses, or devices based on superconducting wires and Josephson junctions.

It may be useful to incorporate these structures into conventional microelectronics and to integrate them with traditional lithographic technology. The arrays of semiconductor and/or metal nano-wires can be used to create 2-D matrices either of conventional p-n, hetero- or Schottky diodes with in-wire junctions [40] which would benefit simply from their reduced dimensions, or of a new variety of "point-contact" diodes with quasi-0 to 3-D junctions between the wire ends and a semiconductor layer deposited on top of the array, with the possibility of either a 2-D barrier or an "inversion shell" layer between them. The first attempt to fabricate such a metal-semiconductor anti-dot array from Ni nano-wire templates produced structures with a complex but interesting  $I$ - $V$  behavior including periodic and anomalous conductance oscillations at room temperatures as mentioned in the previous section.

What we have outlined is a preliminary and, therefore, incomplete account of the possibilities which are potentially opened up by the nonlithographic method for fabricating nano-structured nano-materials and nano-sized elements described above, mainly in the area of solid-state physics and electronics. Other ideas for their application both in science and industry will undoubtedly emerge as this fabrication technology evolves to include the production of highly-ordered, defect-free nanostructures with controllable parameters.

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**Jimmy M. Xu** (M'87-SM'91) for a photograph and biography, see p. 1620 of this issue.