

NONLITHOGRAPHIC FABRICATION AND COLLECTIVE BEHAVIOR FOR FUTURE NANOELECTRONICS AND COMPUTATION

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1. Introduction

The great success of microelectronics has occurred, not due to radical technological revisions during its evolution, but due to the remarkable performance improvements enabled by miniaturization. Few, if any, fundamental changes have been made to the planar process of Noyce from 1958 and the MOS transistor scaling ideas proposed in the early 1970s¹—they have instead been refined to an unprecedented level. Despite its undeniable success, the microelectronics industry is reaching a crossroads. Previously routine semiconductor process improvements now demand serious or even heroic research, development and investment, and fabrication plants now cost billions of dollars to build². In fact, marching in parallel with the famed Moore's law, which correctly predicted the doubling of semiconductor system performance every 18 months, has been a less discussed but equally important law on the economic side: the capital investment for the equipment and research required to fuel Moore's law also doubles every generation³.

This economic law suggests that even if basic physical and technological problems are surmountable, the semiconductor industry will be first forced to address the exploding costs of research and equipment and to balance them against the diminishing benefits realized by following the one-dimensional track of miniaturization. As costs increase exponentially while return-on-investment in hardware technology decreases, all but the largest players will be squeezed out, and capital will flow to the areas in which radical innovation and significant performance improvement are still possible: *e.g.* novel silicon architectures, system designs, and software. This will consequently slow down innovation in hardware technologies and lead to the plateauing of Moore's law.

Thinking optimistically, the saturation of Moore's law may still be a blessing in disguise. Since no one can predict the final outcome as hard economic and technical limits are reached over the next two decades, the future of computing need not be determined exclusively by the major players in the industry, or others with billions of dollars to invest. Instead, one can anticipate an explosion in creativity—new device, architecture and system designs—that will be required to address the burgeoning problems arising from miniaturization, interconnection and heat dissipation. The search for alternative paths to nanoelectronics opens up the future to many more potential players, and likely new ones as well.

Alternatives to the well-trodden path of miniaturization do exist. Nonlithographic nanofabrication is one example—a particularly attractive one given that lithography is the most costly part of the current technology. It is becoming increasingly apparent that “natural” approaches—*e.g.* self-organization and/or self-assembly—can produce regular, well-ordered, high quality structures on the scale of nanometers. In such fabrication processes, physical and chemical laws, acting and/or competing on small characteristic length scales, conspire to build or “grow” structures at the nanometer scale. Such approaches typically require relatively little human intervention in comparison to photo or electron beam lithography (Section 2).

Indeed, it is possible that while circumventing some of the difficulties faced by lithography, non-lithographic nanofabrication techniques can also address some of the most significant problems facing current and near-future microelectronic systems: wiring, heat dissipation, and quantum effects.

In order to keep the resistance of circuit interconnects low, it is desirable to make them as broad as possible. However, this requirement contradicts the philosophy of miniaturization, which improves the functionality and power of semiconductor systems and devices by increasing packing density. While research laboratories may achieve the routine production of sub-100 nm minimum feature sizes⁴, interconnecting these devices to form useful multi-million transistor circuits is a serious challenge with no immediate solution. Indeed, we are on the verge of observing fascinating but undesirable physical effects such as conductance quantization and ballistic transport in VLSI interconnects. Such wires are no longer passive lines of connection, but instead participate in nonlinear processing of digital signals, and should be regarded more as functional devices, thus rendering invalid current circuit design methodologies based on existing connectivity theory.

Moreover, the total wiring length per unit area in modern microprocessors is now on the order of kilometers per square centimeter. While such numbers are a testament to impressive engineering, it is not clear how much this can be increased, nor what the associated performance improvements or trade-offs will be. Advances such as IBM’s highly publicized copper interconnect process⁵, while important on the scale of years and months, represent one-time, evolutionary changes to an existing technology, and not the revolutionary changes which will be required to guide microelectronics through the next few decades.

With today’s fastest processors dissipating approximately 30 W cm^{-2} —more than a typical cooking element—heat dissipation will become an even greater problem as packing density continues to rise⁶. There is certainly room for improvement—modern day microprocessors dissipate approximately 10^{-6} J per bit switched, while the human brain is estimated to dissipate only 10^{-16} J per bit⁷. In view of these numbers, it will be less and less viable to charge up increasingly narrow and resistive RC transmission lines to communicate between logic blocks. “Wireless” computing alternatives, such as those which depend on electronic polarization of nanostructures, may have an advantage in solving this problem, since little

current—and hence almost no Joule heating—is associated with signal transmission⁸.

Yet another looming problem which will affect future generations of deep-submicron circuits is the failure of the fundamental assumptions underlying the semi-classical Boltzmann transport equation—a direct consequence of the success of miniaturization⁹. As device dimensions drop below the dephasing length and/or the mean free path of the electron (>100 nm in high-quality semiconductors), we enter the realm of quantum transport. In this regime, the phase of the electron wavefunction becomes relevant, and phenomena such as ballistic transport, coherent interference and reflection have observable effects. At still smaller size scales (~1 nm), quantum tunneling (*e.g.* through thin transistor gate oxides) also becomes significant. All of these miniaturization effects disrupt many of the most fundamental design demands of digital systems such as signal cascadability, fan-out, binary logic restoration, and input-output isolation.

As minimum feature sizes continue to decrease, fabrication reliability also grows less and less certain, since statistical averaging over decreasing numbers of dopants and other impurities implies increasing relative deviations. Therefore, as device counts on a chip rise via miniaturization (and increasing die area), the performance deviations scale up inversely with decreasing device volume, and hence the yield of defect-free chips decreases dramatically. The issue of hardware based fault-tolerance then becomes important, and indeed it may no longer be technically or economically feasible to demand defect-free chips. The “Teramac” project at Hewlett-Packard¹⁰ is an example of one massively parallel computer architecture initiative intended to address these problems. Such a system demonstrates that a properly designed system architecture can circumvent the imperfect yield of devices, and suggests that the presence of defects in self-organized nanosystems need not interfere with their potential utility as computational machines.

We envision a goal of computing using non-lithographic and/or self-organized nanostructures, although not by attempting to implement VLSI on a smaller scale with new nanodevices—*i.e.* not by simply continuing to exploit the heretofore successful paradigm of miniaturization. The advanced state of the art in VLSI design and layout principles, the high degree of refinement of the existing devices, and the problems presented by mesoscopic physical effects suggest that a radically different design approach will be required to realize any advantage over existing technologies and methods. Another more fundamental reason for employing a different approach is that we give ourselves the opportunity to exploit directly the physics of nanostructures, rather than merely tolerating such effects as silicon VLSI must do. Consequently, any study of potential applications of coupled nanoarrays must begin with the basic physics of electronic transport in the nanostructures, and with the physics of interactions between individual elements. In fact, we will argue that the symmetric and long-range coupling between nanostructures in an array raises the possibility of engineering a neural network or cellular automaton-like system to solve hard computational problems through the collective behavior in the array (Sections 3, 4). Such a system would encode a

massively parallel computer directly in a physical system, and would compute through the physics of the interactions between individual elements, circumventing the problem of interconnection and possibly that of the power dissipation associated with binary switching.

Despite such fascinating possibilities, there exist numerous challenges to the development of devices and systems based on non-lithographic nanostructures. At the present time, a VLSI microprocessor is a physical system with a phenomenal degree of complexity or information content. Present day nanostructured materials tend either to be randomly patterned, or ordered but in too small a number, or else to have a very simple lattice structure repeated many millions of times (Section 2)—neither a random (amorphous) lattice nor a regular lattice replicates the engineered complexity of a microprocessor. Therefore, while the opportunities are great, challenging work lies ahead.

The organization of the paper is as follows: in Section 2 we survey a number of techniques of non-lithographic fabrication of nanostructures, but principally our preferred method of nano-fabrication using an anodic aluminum oxide (AAO) template; in Section 3 we describe some of the novel physics predicted to occur in close packed nano-arrays and motivate future device and system applications; in Section 4 we describe our nanostructures in the context of potential neural computation systems; finally in Section 5 we present our conclusions.

2. A Survey of Techniques for Nanofabrication

The principal methods for fabricating nanomaterials developed so far include conventional photolithography-based techniques¹¹, direct-write electron-beam lithography^{12,13}, self-assembling or self-organizing nanoparticles or quantum dots¹⁴, sol-gel processing^{15,16}, nanochannel glass (NCG) templates¹⁷, electroplating of polycarbonate membranes¹⁸ and anodic aluminium oxide (AAO) templates¹⁹.

The fabrication of structures with feature sizes smaller than 100 nm is an expensive and technically daunting task using conventional (e-beam and photo) lithographic methods. Therefore, it is natural to seek other possible fabrication techniques—nonlithographic methods—which may be better suited for mass production of nanoscale devices. Most approaches fall into one of three main categories: (i) template methods; (ii) self-organized nanostructures; and (iii) direct growth. In this discussion, we will focus primarily on the nanotemplate approach using anodic alumina, but will describe briefly a number of different approaches. We will also mention some hybrid methods which incorporate a lithographic step into their process.

2.1 Formation of nanotemplate and nanostructure arrays

Porous aluminium oxide films formed by electrochemical anodization processes in various electrolytes have been studied for more than 40 years²⁰. This technique has been widely used by industry for aluminium surface coloring. Anodic porous alumina can be fabricated to exhibit a packed array of columnar hexagonal cells

with cylindrical, uniformly sized pores ranging from 4 nm to 200 nm in diameter. The diameter and length of the pore may be controlled by selecting the electrolyte composition and concentration, and the anodization voltage and time. The main mechanism leading to straight and uniform pore formation is believed to be the field-assisted dissolution of the oxide²¹.

This technique was recently observed by Masuda *et al.* to produce a highly ordered, hexagonal close-packed “honeycomb” structure under appropriate processing conditions²². The mechanism of forming the highly ordered self-organized structure is not yet fully understood, although some recent work has investigated the process^{23,24}. The ordering structure was found to be strongly effected by the cell voltage. A regular honeycomb structure with high aspect ratio has been obtained by mechanical patterning of the surface followed by anodization²⁵, and by a two-step anodization process²⁶. Figure 1 shows a SEM image of a typical example of the self-organized anodic alumina template with highly ordered pores, recently fabricated by the authors.

After fabricating the AAO template, nanostructures may be grown in the pores by a number of different methods: (i) Electrochemical deposition of metals, alloys and compounds into the pores of the template²⁷; (ii) Electrophoretic filling of the pores with colloids²⁸; (iii) Filling with sol gel via capillary action or with metals at high pressure²⁹; (iv) Filling through CVD or polymerization^{30,31}.

Electrochemical deposition of metals in the AAO template has been used to produce nano-wire arrays with interesting magnetic and optical properties, differing from those of the bulk materials²⁷. Additionally, A^{II}B^{VI} compounds (*eg.* CdS and CdS_xSe_{1-x}) have been deposited into the AAO template³². Gold clusters and colloids (quantum dots) have been introduced into the AAO template via electrophoresis²⁸. Finally, bismuth quantum wire arrays have been deposited by a vacuum melting and pressure injection process²⁹. Li *et al.* developed a method for first producing (Figure 2(a)-(c)) and subsequently filling arrays of carbon nanotubes in the AAO template (Figure 2(d))³⁰. The desired interior metal, such as nickel or cobalt, was deposited within the nanotubes by electroless deposition.

The AAO template nanofabrication method possesses many advantages. It provides a simple and inexpensive way to fabricate large area, highly ordered, high density (10^{11} cm⁻²) arrays of close packed nanopores that can be filled with wires, dots and even tubes in a large range of materials. Magnetic and non-magnetic metals, superconductors, semiconductors, other optical materials, and, recently, carbon nanotubes, have all been successfully deposited.

The potential applications for such a technology are numerous, and include ultra-high density magnetic storage, field-emission displays, and optical/infra-red detectors. These possibilities have been described in the literature³³. The recent progress in forming highly ordered and uniform array structures makes these possibilities all the more promising.

2.2 Other non-lithographic nanofabrication techniques

There currently exist a large number of techniques for the fabrication of nanometer scale structures, one class of which we have described above. Other template based techniques include: track etch membranes, in which polycarbonate or polyester templates are bombarded with nuclear fission products and then etched to create channels in the damaged regions; mesoporous or molecular templates such as zeolites, molecular sieves and other materials³⁴; nanochannel glass arrays, in which glass fibers with etchable cores are packed together and drawn repeatedly at high temperature, leading to nanometer scale cores which are then etched away³⁵. Many approaches exist for filling the voids in the templates with different materials.

Self-organized growth of nanostructures is another popular approach, principally via the Stranski-Krastanow semiconductor growth mode³⁶ in which nanoscale islands form during the growth of highly strained layers. Finally, direct-write nanofabrication methods have been developed using scanning probe microscopy³⁷, and atom lithography employing the standing wave pattern of a laser³⁸.

Many of the methods outlined above can be used in conjunction with conventional lithographies. For example, templates and self-assembled nanostructures can be used as lithographic masks. Additionally, the mechanical patterning of substrates using nanotemplates formed via EB lithography prior to self-assembly or anodization can lead to a much higher degree of ordering. It is desirable in these cases that any serial lithographic step be used only once, *e.g.* to form a mask. A hybrid method of microcontact printing was used by Whitesides *et al.* to stamp patterned self-assembled monolayers onto a substrate which was then etched to transfer the pattern onto the substrate³⁹. A unique feature of this method is its ability to produce nanostructures on curved surfaces. Using a similar technique Pang *et al.* have been able to press a wide variety of nanopatterns onto the surface of aluminum⁴⁰.

3. Cooperative phenomena and collective excitations in nanosystems

There are a number of surprising and interesting phenomena which arise in the study of nanostructures, many of which are associated with their interactions and collective behavior. In this section we discuss some of the theoretical investigations and considerations arising from the study of close-packed nanoarrays, and motivated by the prospect of novel computational architectures and/or methodologies.

On the nanoscale, statistical approximations commonly used in macroscopic physics lose validity as the “granularity” of atoms and electrons becomes apparent. As a result, such phenomena as electronic screening, electronic band formation, electron-phonon interaction etc. exhibit peculiarities which are absent in “orthodox” solid state physics. A remarkable example are carbon nanotubes: These nanostructures exhibit a drastic modification of the band structure with a simple change of the nanotube diameter⁴¹. It has been predicted theoretically⁴² and then experimentally confirmed^{43,44} that single-walled carbon nanotubes can

exhibit both semiconductor and metallic behavior depending on the nanotube helicity. On the other hand, multi-walled nanotubes display behavior characteristic of amorphous carbon⁴⁵ with a consequent electron-phonon coupling and a possible lattice softening coming into effect⁴⁶.

One can anticipate the appearance of nontrivial cooperative phenomena due to a superstructure formation in the case of nanostructures formed in a periodic array; systems of this type have already been studied in the literature⁴⁷. A spontaneous polarization in 2D array of quantum dots was predicted to yield a ferroelectric-like phase transition^{48,49}. A ferroelectric transition in a molecular-like 2D array of quantum dots has also been predicted, with a double-well anharmonic rather than quadratic confinement potential being inherent for every double-dot “molecule”⁵⁰. If we change from 0D (“dot-like”) to 1D (“wire-like”) objects the cooperative behavior of such arrays can also have an important potential role in developing novel computational hardware and/or algorithms reminiscent of cellular automata and neural networks⁵¹. For example, let us consider an array of vertically-oriented quantum wires placed between top and bottom electrodes. For individual wires with the Coulomb interaction the charge density distribution was shown⁵² to differ strongly from that obtained for the conventional Luttinger liquid model. The charge density rapidly decays from the ends to the middle of the wire, with an exponential cutoff at ($\hbar = 1$), $l \sim \frac{a}{e} \sqrt{\epsilon v_f}$

where a is the wire lattice parameter, v_f is the Fermi velocity, and ϵ is the dielectric constant of the medium surrounding the wires. Thus, in the case of an array, where the interwire distance is sufficiently large compared to the length of a nanowire ($d \gg L$), we have an interacting array of dipoles. The peculiarity of this system lies in the competition between two tendencies: the external bias tends to maintain ferroelectric order whereas the dipole-dipole interaction promotes the antiferroelectric arrangement. With respect to low-energy excitations the system may be treated as a 2D system of Heisenberg spins in an external magnetic field (bias)⁵³, known to describe the formation of ferromagnon-like quasiparticles which can thus propagate through the dipole array.

At zero applied bias the fluctuations of electron density can cause spontaneous dipole formation. Let us set the probability of a dipole formation at the site i as χ_α^i , where the index $\alpha = 1, 2$ corresponds to different dipole orientations. The increment in the energy of the array due to formation of a dipole is

$$\Delta E = \sum_{i,\alpha} E_i \chi_\alpha^i - \frac{1}{2} \sum_{i,\alpha} \sum_{j,\beta} J_{ij}^{\alpha\beta} \chi_\alpha^i \chi_\beta^j$$

where $J_{ij}^{\alpha\beta}$ is the interaction energy. The energy of an individual dipole E_i depends on the scale of charge fluctuations q . In the mean field approximation $x_1 = \langle \chi_1^i \rangle$, $x_2 = \langle \chi_2^i \rangle$ and the energy increment per site is reduced to⁵⁴

$$\Delta E' = \bar{E}(x_1 + x_2) - \frac{1}{2} V(x_1^2 + x_2^2) + W x_1 x_2$$

where $V = V(n)$ corresponds to a self-action, $W = W(n)$ is an effective interaction between the dipoles of different orientation, and $n = q/e$ is the measure of charge fluctuation. The change of configurational entropy is found to be

$$\Delta S = \log \left[\frac{\sigma^{N(x_1+x_2)} N!}{(x_1 N)! (x_2 N)! (N(1-x_1-x_2))!} \right]$$

where N is the number of wires in the array and $\sigma = (2n)! / (n!)^2$ accounts for the degeneracy of a particular charge state. The equilibrium values of x_1 and x_2 are associated with a minimum in the increment of free energy, which yields

$$2\sigma \frac{1-\xi}{\sqrt{\xi^2 - \eta^2}} = \exp(\alpha - \gamma\xi/2), \quad \frac{\xi + \eta}{\xi - \eta} = \exp(\beta\eta)$$

where $\xi = x_1 + x_2$ is the concentration of dipoles, $\eta = x_1 - x_2$ is the total polarization, $\alpha = \bar{E}/T$, $\beta = (W + V)/T$, and $\gamma = (W - V)/T$ ($k_B=1$). From the above one obtains:

$$\xi = \frac{1}{\beta} \frac{\zeta + 1}{\zeta - 1} \log(\xi)$$

where

$$\zeta = -1 + \frac{1}{2} \delta^2 \left[1 - \sqrt{1 - (2/\delta)^2} \right], \quad \delta = \frac{1}{\sigma} \frac{\xi}{1-\xi} \exp(\alpha - \gamma\xi/2)$$

The graphical solution of the equation defining ξ is shown in Figure 3 for several different values of $W = V = \bar{E}/2$. The transition to the polarized state with change in interaction parameter values is manifested as a jump in the equilibrium value of dipole concentration ξ from zero to $\xi \sim 0.8$.

In the dipole model of close-packed nanowire arrays, we see many analogies with cellular automata—*i.e.*, the state of a given cell (or dipole, or nanowire) is determined partly by global external forces—an external voltage bias—and partly by the local environment—the state of adjacent dipoles. Such interactions in the context of cellular automata and also neural networks are the subject of much research effort in computer science. While current computer systems implement these models entirely in software, with some effort made on the architecture level, a computer based on the physics of interacting dipoles would solve such problems directly through massively parallel physical interactions, and much more rapidly than software running on conventional computer systems.

4 Computation schemes employing ordered nano-arrays

Though the sequential binary processing paradigm used in existing computers was formulated by von Neumann, it is interesting to note that in some of his later publications, he took a radically different direction from his previous work⁵⁵. He had grown interested in a form of massively-parallel distributed computation, inspired by the remarkable computations performed by the human brain. This computational architecture is premised on the idea that a variety of sophisticated

computations may be performed by a large coupled array of simple computational elements obeying basic rules of behavior—an ideal opportunity for the densely packed, ordered nano-arrays which we are now able to fabricate. The computational potential of such systems for particular classes of problems was recognized early on by Hopfield⁵⁶.

4.1 Potential advantages of physical massively parallel computation

Distributed computational systems are known for their ability to solve rapidly difficult computational problems such as pattern recognition or path optimization (*e.g.* “travelling salesman”) through massively parallel operation of (possibly slow) computational elements. Such systems are also fault-tolerant due to their “graceful” degradation with the failure of individual computational elements. Fault-tolerance is an important consideration in view of the imperfect statistical yield of nanoscale components and systems produced by both conventional lithography and by non-lithographic means (Section 1). Thus, massively parallel, neural computing is the approach to computation naturally suited for building computers from self-organized, non-lithographic nanomaterial systems.

4.2 Computation as evolution of phase space trajectory

In seeking novel computational capabilities derivable from ordered nanoarrays, it is useful to examine a generalized picture of computational machines. We describe a computational machine by a space of states and system dynamics acting in the space. Each state vector contains all relevant information about the system, including the state of all computational elements, memory elements, inputs, and outputs. The system dynamics describe the evolution of the computer from one state to the next. Computations are therefore represented as trajectories in a state space or phase space. We restrict ourselves to systems where the dynamics are deterministic, treating noise as a stochastic perturbation to the state of the system.

For example, in this framework, the digital computer is a machine having a discrete state space and discrete dynamics, iteratively mapping the state f_i to the state f_{i+1} until a stable point (solution) is reached. Computation is performed by the deterministic transition from one state to the next, ultimately mapping every initial (input) state to a final (output) state. The discreteness of the state space arises from logic level restoration, a fundamental requirement of digital computation, which restores state information to the nearest grid point.

In contrast, the distributed computer possesses a continuous state space (with dimension equal to the number of computational elements) and a differential dynamics over that space. Again, computation is embodied in the evolution of the system state: *i.e.* in the mapping formed between initial and final states. For this computational machine to be capable of rejecting noise—the stochastic perturbation of the system state to some neighboring state—adjacent initial states $f(x)$ and $f(x+\delta)$ must result in identical outputs. In other words, this demands differential stability for all state space trajectories. Conveniently, this constraint

and its implications have already been studied in detail in the work of Hopfield, thus providing a foundation for the study of computational systems of the type examined here.

4.3 First order dynamics of computational machines

Although the physical system implementing the desired computational machine may be quite complex, it is often sufficient, and certainly illustrative, to model it as an array of interacting first-order elements. In the language of neural networks, we define S_i as the state of element i , as determined by the value of some observable quantity, and q_i as its activation potential, representing an internal parameter more directly related to the inputs to i . In general, the inputs to an element represent the collective influence of other computational elements in the array combined with a possible external force. The state S_i and the activation potential are related by $S_i = \Phi_i(q_i)$ where the function Φ_i is termed the activation function. Φ_i is often required to be monotonic, but need not be identical for all computational elements. The continuous-time deterministic system is then guided by the dynamics given by

$$C_i \frac{dq_i}{dt} = \sum_j w_{ij} s_j - R_i q_i - \theta_i$$

where C_i represents the response time of the element (*i.e.* capacitance), R_i is a gain parameter, θ_i is the external input to the element, and w_{ij} is the weight for coupling element i to element j . The steady state solution of this equation reveals that the activation potential of an element is determined by a weighted linear superposition of the internal and external inputs.

The stability condition necessary for noise rejection in the distributed processor takes a simple form in this context, requiring that there be symmetric coupling between the elements, *i.e.* $w_{ij} = w_{ji}$. Furthermore, this coupling symmetry, which is fortunately the rule rather than the exception in physical systems, dictates that the computational trajectories are the gradients of the energy function given by⁵⁷

$$E = - \sum_{i \neq j} w_{ji} s_i s_j + \sum_{j=1}^N \frac{1}{R_j} \int_0^{s_j} \varphi_j^{-1}(s_j) ds_j + \sum_{j=1}^N \theta_j s_j$$

Similar results can be obtained for more general systems, including those for which the dynamics contain a stochastic (thermal) character. Such an energy function is reminiscent of that describing an array of dipoles as discussed in Section 3.

Relations such as the above also arise in statistical mechanics where they serve as the basis for the study of phase transitions and co-operative phenomena⁵⁸. It is nevertheless an open question as to whether such relations can be used to obtain non-trivial computational functions from existing, controllable physical systems. This issue has been addressed by neural network researchers, albeit from the opposite direction: *viz.*, seeking a *model* system in which to implement a computer and then creating (discovering) the symmetrically coupled array through the process of training.

4.4 Neural networks and self-organized nanostructure arrays

Pursuing further the analogy with neural network theory, we inherit a road map for applications, approaches, and potential pitfalls. From work on the Hopfield machine come applications in error correction, associative memory, energy minimization, and an awareness of the problems presented by spurious local minima in the energy surface. In the Boltzmann and mean-field-theory machines we find an example of traditional input-output based computing, as well as a guide to non-zero-temperature computation⁵⁹.

The analogy with neural networks is not a perfect one. Considerable work in neural network theory is concerned with network training—that is, adjusting the weights w_{ij} of the connections based on the difference between two solutions to a representative problem: that obtained by the network, and the correct solution. The practical difficulties associated with training have seriously limited the popularity and applicability of this computational approach. In the case of ordered nanoarrays, however, the inter-element weights or couplings may be fixed by the morphology of the structure, in which case the system could not be trained in the conventional sense. Nevertheless, a non-adaptive machine based on such a system can still offer many advantages including low power consumption, fault tolerance, and possibly wireless implementation; the set of problems solvable by such a system is, of course, reduced.

Although neural network theory usually favors adjustment of the weights w_{ij} , neglecting the possibility of adjusting individual (nonlinear) activation functions, $\Phi_i(q_i)$, the latter is actually a much more attractive technological possibility with our own system. For example, selectively loading nanopores with different materials could alter the conductivity of the nanowires, or the response of their polarization to external influences; a lithographic writing step could produce contacts to separately bias certain individual nanowires or small regions of the array. In general, some activation functions could be temporarily or permanently differentiated from others. These are some possible avenues for engineering complexity into the array, thereby enabling specific problems to be computed, or a generalized computing architecture to be built. With increasing control over the fabrication of individual nanostructures, more general and powerful functions will be possible.

Uniformity and/or symmetry in the array is both a limitation and a potential strength—while lattice translation symmetry indicates low information content, it also represents an opportunity for the creation of powerful and flexible systems—if the regions of the array may be dynamically differentiated from others (*e.g.* via charging or polarization), it may be possible to create/program a computer “on the fly” which will solve a given computational problem, to read the result, and then to generate immediately a different computer for the next problem. Such speculations presuppose a very high degree of control over the writing and reading of different states to and from the individual elements of the array, and obviously demand extremely fast, high bandwidth communication capability to

simultaneously program arbitrary states into all elements of the array. While highly speculative at the present time, these objectives could be seen as the ultimate long-term goals for the nanocomputational architect or system designer—to step out of the way of the physics as much as possible, and let computation proceed via fast and fundamental processes.

5 Conclusions

Miniaturization is the primary source of the remarkable applications enabled and created by microelectronics. However, because microelectronics still operates according to VLSI design rules premised on macroscopic physics, it is ill equipped to deal with the sub-100 nm realm. Even if the technical challenges can be overcome, the economics of Moore's law are becoming increasingly unattractive. Since the SIA roadmap predicts minimum feature sizes on the 100 nm scale within the next ten years, it is important to study potential successor technologies. These technologies, instead of merely dealing with the problems associated VLSI miniaturization, can instead be designed from the ground up to embrace and exploit the fundamental physics of electrons and atoms on the nanoscale. Based on their low cost, high manufacturing throughput, and material versatility it is non-lithographically fabricated nanosystems will spawn such technologies, which will require new architectures incorporating fault tolerance, high interconnection, and possibly a neural network approach rather than serial binary logic. However, the cooperative behavior and collective phenomena of self-organized nanodevice arrays are shown to be compatible with these basic requirements. While the challenges facing the implementation of such technologies are significant, we must remember that no one (except for Gordon Moore) predicted the pace of evolution in planar integration even after several years of development. Who can say now what the future holds for non-lithographic nanosystems, or what applications they might enable?

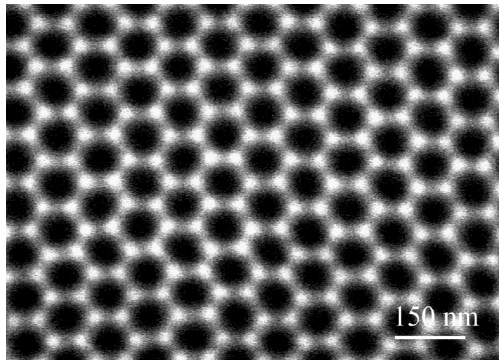


Figure 1. Ordered AAO nanotemplate exhibiting hexagonal close-packed lattice.

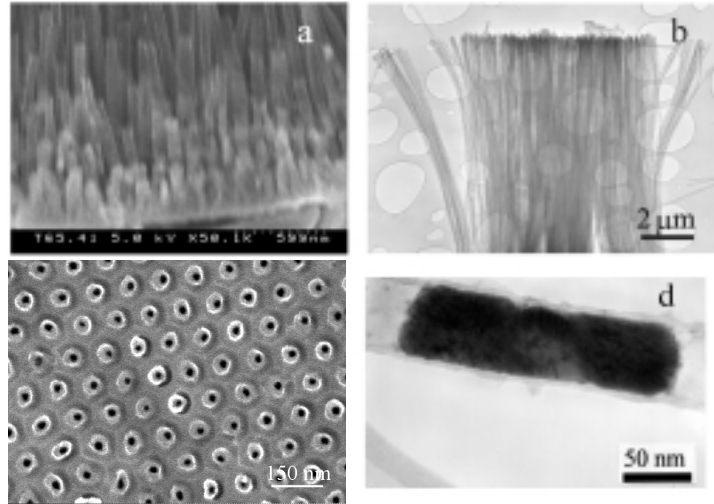


Figure 2. (a) SEM image of carbon nanotubes partially exposed by etching the AAO template with NaOH; (b) TEM image of free carbon nanotube bundle after long etching; (c) SEM top view of exposed nanotubes; (d) TEM image of a P-doped Ni particle deposited in the interior of a carbon nanotube.

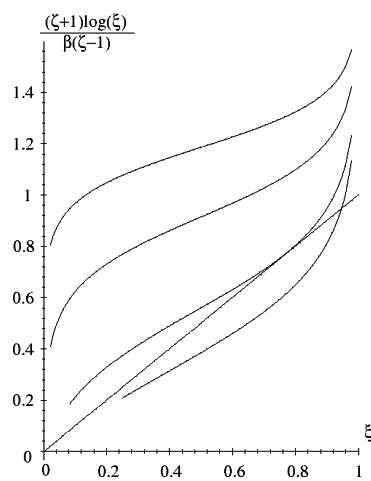


Fig. 3. Plot of the equation for ξ , showing the transition to a polarized state indicated by a jump in equilibrium ξ . The parameter values are $n = 7, W = V = \bar{E}/2 = 20, 15, 11.3, 10$.

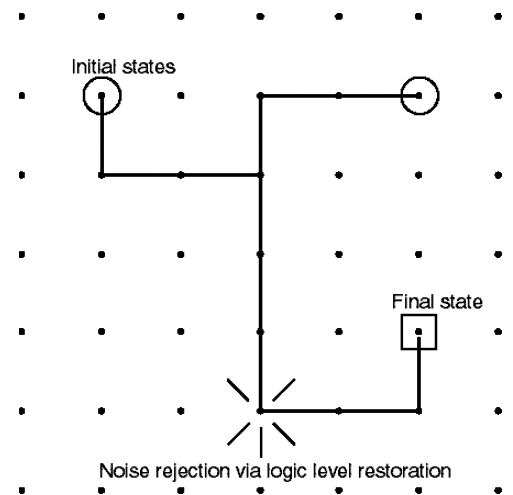


Figure 4. Abstract representation of a digital computer showing binary level restoration (noise rejection). The analog (distributed) computer operates in an identical manner in a continuous state space.

References

- ¹ B. Hoeneisen and C. Mead, "Fundamental limitations in microelectronics. I. MOS technology", *Solid State Electron.* **15**, 819, 1972; R. H. Dennard, F. H. Gaensslen, H. N. Yu *et al.*, "Design of ion-implanted MOSFET's with very small physical dimensions", *J. Solid State Circ.*, **SC-9**, 256 (1974).
- ² Semiconductor Industry Association, *The National Technology Roadmap for Semiconductors* (SIA: San Jose, 1997).
- ³ M. S. Malone, *The Microprocessor: A Biography* (Springer-Verlag: New York, 1995).
- ⁴ See, *e.g.*, H. Kawaura, T. Sakamoto, T. Baba, *et al.*, "Transistor operation of 30-nm gate-length EJ-MOSFET's", *IEEE Electron Dev. Lett.*, **19**, 74 (1998) and references contained therein.
- ⁵ L. Geppert, "The media event: Moore's Law mania", *IEEE Spectrum* **35**, 20 (1998).
- ⁶ R. W. Keyes, "The future of the transistor", *Scientific American* ("Solid – state century", Special Issue) Dec. 1997.
- ⁷ S. Haykin, *Neural Networks: A Comprehensive Foundation* (IEEE Press: New York, 1994).
- ⁸ See, *e.g.*, C. S. Lent and P. D. Tougaw, "Device architecture for computing with quantum dots", *Proc. IEEE* **85**, 541 (1997), and references contained therein.
- ⁹ S. Datta, *Electronic Transport in Mesoscopic Systems* (University Press: Cambridge, 1995); D. K. Ferry and S. M. Goodnick, *Transport in Nanostructures* (University Press: Cambridge, 1997).
- ¹⁰ J. R. Heath, P. J. Kuekes, G. S. Snider, R. S. Williams, "A defect-tolerant computer architecture: opportunities for nanotechnology", *Science* **280**, 1716 (1998).
- ¹¹ F. Burmeister, C. Schaffe, B. Keilhafer *et al.*, "From mesoscopic to nanoscopic surface structures; Lithography with colloid nanolayers", *Adv. Mater.* **10**, 495 (1998).
- ¹² S.Y. Chou, P. R. Krauss, and L. Long, "Nanolithographically defined magnetic structures and quantum magnetic disk", *J. Appl. Phys.* **79**, 6101 (1996).
- ¹³ S.Y. Chou, P. R. Krauss, M. S. Wei, and P. B. Fischer, "Nanolithographically defined magnetic structure", *Scr. Metall. Mater.* **33**, 1537 (1995).
- ¹⁴ R. Notzel, "Self-organized growth of quantum-dot structures", *Semicond. Sci. Technol.* **11**, 1365 (1996).
- ¹⁵ D. Levy and L. Esquivias, "Sol-gel processing of optical and electrooptical materials", *Adv. Mater.* **7**, 120 (1995).
- ¹⁶ B. B. Lakshmi, C. J. Patrissi, and C. R. Martin, "Sol-gel template synthesis of semiconductor oxide micro- and nanostructures", *Chem. Mater.* **9**, 2544 (1997).

- ¹⁷ P. P. Nguyen, D. H. Pearson, and R. J. Tonucci, "Fabrication and characterization of uniform metallic nanostructures using nanochannel gas", *J. Electrochem. Soc.* **145**, 247 (1998).
- ¹⁸ V. M. Cepak, J. C. Hulteen, G. Che, *et al.*, "Chemical strategies for template synthesis of composite micro- and nanostructures", *Chem. Mater.* **9**, 1065 (1997).
- ¹⁹ D. Routkevitch, A. A. Tager, J. Haruyam *et al.*, "Nonlithographic nano-wire arrays: fabrication, physics, and device applications", *IEEE Trans. Electron Dev.* **43**, 1646, (1996).
- ²⁰ F. Keller, M. S. Hunter and D. L. Robinson, "Structural features of oxide coatings on aluminum", *J. Electrochem. Soc.* **100**, 411 (1953).
- ²¹ J. P. O'Sullivan and G. C. Wood, "The morphology and mechanism of formation of porous anodic films on aluminum", *Proc. Roy. Soc. Lond. A.* **317**, 511 (1970).
- ²² a) H. Masuda and K. Fukuda, "Ordered metal nanohole arrays made by a two-step replication of honeycomb structures of anodic alumina", *Science* **268**, 1466 (1995); b) H. Masuda, F. Hasegawa, S. Ono, "Self-ordering of cell arrangement of anodic porous alumina formed in sulfuric acid solution", *J. Electrochem. Soc.* **144**, L127 (1997).
- ²³ O. Jessensky, F. Muller and U. Gosele, "Self-organized formation of hexagonal pore arrays in anodic alumina", *Appl. Phys. Lett.* **72**, 1173 (1998).
- ²⁴ L. Zhang, H. S. Cho., F. Li, R. M. Metzger and W. D Doyle, "Cellular growth of highly ordered porous anodic films of aluminium", *J. Mat. Sci. Lett.* **17**, 291 (1998).
- ²⁵ H. Masuda, H. Yamada, M. Satoh *et al.*, "Highly ordered nanochannel-array architecture in anodic alumina", *Appl. Phys. Lett.* **71**, 2770 (1997).
- ²⁶ H. Masuda and M. Satoh, "Fabrication of gold nanodot array using anodic porous alumina as an evaporation mask", *Jpn. J. Appl. Phys.* **35**, L126 (1996).
- ²⁷ D. AlMawlawi, N. Coombs, and M. Moskovits, "Magnetic properties of Fe deposited into anodic aluminum oxide pores as a function of particle size", *J. Appl. Phys.* **70**, 4421 (1991).
- ²⁸ G. Hornyak, M. Kroll, R. Pugin, *et al.*, "Gold clusters and colloids in alumina nanotubes", *Chem-Eur. J.* **3**, 1951 (1997).
- ²⁹ Z. Zhang, J. Y. Ying and M. Dresselhaus, "Bismuth quantum-wire arrays fabricated by a vacuum melting and pressure injection process", *J. Mater. Res.* **13**, 1746 (1998).
- ³⁰ J. Li, M. Moskovits, and T. L. Haslett, "Nanoscale electroless metal deposition in aligned carbon nanotubes", *Chem. Mater.* **10**, 1963 (1998).
- ³¹ R. V. Parathasarathy, K. L. N. Phani, and C. R. Martin, "Template synthesis of graphitic nanotubules", *Adv. Mater.* **7**, 896 (1995).
- ³² D. Routkevitch, T. Bigioni, M. Moskovits and J. M. Xu, "Electrochemical fabrication of CdS nanowire arrays in porous anodic aluminum oxide templates", *J. Phys. Chem.* **100**, 4037 (1996).
- ³³ A. A. Tager, D. Routkevitch, J. Haruyama *et al.*, "Nonlithographic fabrication and physics of nanowire and nanodot array devices – present and future", in *Future Trends in Microelectronics*, S. Luryi, J. M. Xu and A. Zaslavsky, eds. (Kluwer: Norwell, 1996).

- ³⁴ G. A. Ozin, "Nanochemistry: Synthesis in diminishing dimensions", *Adv. Mater.* **4**, 612 (1992).
- ³⁵ R. J. Tonucci, B. L. Justus, A. J. Campillo and C. E. Ford, "Nanochannel array glass", *Science* **258**, 783 (1992).
- ³⁶ R. Leon, P. M. Petroff, D. Leonard and S. Fafard, "Spatially resolved visible luminescence of self-assembled semiconductor quantum dots", *Science* **267**, 1966 (1995).
- ³⁷ T. A. Jung, R. R. Schlittler, J. K. Gimzewski, H. Tang and C. Joachim, "Controlled room-temperature positioning of individual molecules: Molecular flexure and motion", *Science* **271**, 181 (1996).
- ³⁸ R. E. Scholten, J. J. McClelland, E. C. Palm, A. Gavrin and R. J. Celotta, "Nanostructure fabrication via direct writing with atoms focused in laser fields", *J. Vac. Sci Technol. B* **12**, 1847 (1994).
- ³⁹ G. M. Whitesides, "Self-assembling materials", *Scientific American* **273**, 146 (1995).
- ⁴⁰ S. W. Pang, T. Tamamura, M. Nakao, A. Ozawa and H. Masuda, "Direct nano-printing on Al substrate using a SiC mold", *J. Vac. Sci Technol. B* **16**, 1145 (1998).
- ⁴¹ P. M. Ajayan and T. W. Ebbesen, "Nanometre-size tubes of carbon", *Rep. Prog. Phys.* **60**, 1025 (1997).
- ⁴² C. T. White, D. H. Robertson, and J. W. Mintmire, "Helical and rotational symmetries of nanoscale graphitic tubules", *Phys. Rev. B* **47**, 5485 (1993).
- ⁴³ J. W. G. Wildoer, L. C. Venema, A. G. Rinzler, R. E. Smalley and C. Dekker, "Electronic structure of atomically resolved carbon nanotubes", *Nature* **391**, 59 (1998).
- ⁴⁴ T. W. Odom, J.-L. Huang, P. Kim and C. M. Lieber, "Atomic structure and electronic properties of single-walled carbon nanotubes", *Nature* **391**, 62 (1998).
- ⁴⁵ A. Yu. Kasumov, H. Bouchiat, B. Reulet *et al.*, "Conductivity and atomic structure of isolated multiwalled carbon nanotubes", *Europhys. Lett.* **43**, 89 (1998).
- ⁴⁶ A. Rakitin, M. Ya. Valakh, N. I. Klyui, V. G. Visotski and A. P. Litvinchuk, "Possibility of a double-well potential formation in diamondlike amorphous carbon", *Phys. Rev. B* **58**, 3526 (1998).
- ⁴⁷ R. Landauer, "Self-polarized quantum dots", *Solid State Commun.* **95**, 7 (1995).
- ⁴⁸ K. Kempa, D. A. Broido and P. Bakshi, "Spontaneous polarization in quantum-dot systems", *Phys. Rev. B* **43**, 9343 (1991).
- ⁴⁹ K. Kempa, P. Bakshi, D. A. Broido, *et al.*, "Polarization of electrons in quantum dashes in magnetic field", *Solid State Commun.* **91**, 231 (1994).
- ⁵⁰ A. O. Govorov and A. V. Chaplik, "Ferroelectric phase-transitions in a molecular-like array of quantum dots", *J. Phys.-Condens. Mat.* **6**, 6507 (1994).
- ⁵¹ M. Garzon, *Models of Massive Parallelism: Analysis of Cellular Automata and Neural Networks* (Springer-Verlag: Heidelberg, 1995); S. Wolfram, *Cellular Automata and Complexity: Collected Papers* (Addison-Wesley: New York, 1994).
- ⁵² V. A. Sablikov and B. S. Shchamkhalova, "Coulomb interaction during coherent transport of electrons in quantum wires", *JETP Lett.* **67**, 196 (1998).
- ⁵³ See, *e.g.*, J. M. Ziman, *Principles of the Theory of Solids* (University Press: Cambridge, 1972).

- ⁵⁴ See, e.g., M. E. Lines and A. M. Glass, *Principles and Applications of Ferroelectric And Related Materials* (Clarendon Press: Oxford, 1977).
- ⁵⁵ J. von Neumann, *Theory of self-reproducing automata* (U. of Illinois Press: Chicago, 1966).
- ⁵⁶ J. J. Hopfield, "Neural networks and physical systems with emergent collective computational abilities", *Proc. Nat. Acad. Sci.*, **79**, 2554 (1982).
- ⁵⁷ J. J. Hopfield, "Neurons with graded response have collective computational properties like those of two-state neurons", *Proc. Nat. Acad. Sci.*, **81**, 3088 (1984).
- ⁵⁸ C. Peterson and J. R. Anderson, "A mean-field theory learning algorithm for neural networks", *Complex Systems*, **1**, 995 (1987).
- ⁵⁹ G. E. Hinton and T. J. Sejnowski, in *Parallel Distributed Processing: Explorations in Microstructure of Cognition*, S. J. Hanson J. D. Cowan and C. L. Giles, eds. (MIT Press: Cambridge, 1986).